Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 51. (Cancelled)

52. (Currently Amended) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductive film over a memory cell forming region and a peripheral circuit ~~transistor~~ forming region of a semiconductor substrate;

patterning said first conductive film ~~lying over the~~ in said memory cell forming region to form a first ~~conductive~~ conductor pattern which serves as a first gate electrode of a memory cell; ~~and leaving said first conductive film over said peripheral circuit transistor forming region;~~

forming a second conductive film over said memory cell forming region and over said first conductive film in said peripheral circuit ~~transistor~~ forming region; ~~and~~

etching said second conductive film to form ~~each~~ a second gate electrode of said memory cell on at least side ~~walls~~ surface of said first ~~conductive~~ conductor pattern, and ~~forming a gate~~ to form an electrode structure of ~~each~~ a peripheral circuit ~~transistor~~ element comprising said second conductive film and first conductive film ~~over~~ in said peripheral circuit ~~transistor~~ forming region; and

forming a first silicide layer on said first gate electrode of said memory cell and a second silicide layer on said second gate electrode of said memory cell.

53. (Original) A method according to claim 52,

wherein said memory cell includes, in a memory cell forming region of said semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode and a memory gate electrode disposed over said channel region, a first gate insulating film formed between said channel region and said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

54. (Currently Amended) A method according to claim 53,

wherein said peripheral circuit ~~transistors include~~ element includes a low withstand voltage transistor operated at a power voltage, and a high withstand voltage transistor operated at a voltage higher than said power voltage, and

wherein said first gate insulating film is formed in a gate insulating film forming step for said low withstand voltage transistor.

55. (Currently Amended) A method according to claim 53, wherein said second gate electrode is formed on ~~side walls~~ said side surface of said first gate electrode through an insulating film in sidewall spacer ~~fashion~~ shape.

56. (Original) A method according to claim 53, wherein an electrode withdrawal portion of said second gate electrode is formed in said forming step of the second gate electrode.

57. (Currently Amended) A method according to claim 53, further including a step of patterning said first ~~conductive~~ conductor pattern after said formation of the second gate electrode to thereby form said first gate electrode.

58. – 62. (Cancelled)

63. (Currently Amended) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductive film over a memory cell forming region of a semiconductor substrate and forming an insulating film over said first conductive film;

etching said insulating film and said first conductive film to form a first ~~conductive~~ conductor pattern which serves as a first gate electrode of a memory cell;

forming a second gate electrode of said memory cell on side walls of said first ~~conductive~~ conductor pattern;

removing said insulating film over said first ~~conductive~~ conductor pattern;

forming sidewall spacers, each comprised of an insulating film, in self-alignment with side walls of said second gate electrode; and

forming a silicide layer for each of said first ~~conductive~~ conductor pattern and said second gate electrode in self-alignment with respect to said sidewall spacers.

64. (Original) A method according to claim 63,

wherein in said sidewall spacer forming step, said sidewall spacers are formed on said side walls on both sides of said second gate electrode and side walls of said first gate electrode,

wherein said silicide layer for said second gate electrode and said silicide layer for said first gate electrode are electrically isolated by said sidewall spacer disposed on one side of said both sides,

wherein said silicide layer for said second gate electrode and a silicide layer for a source region or a drain region are electrically isolated by said sidewall spacer on the other side thereof, and

wherein said silicide layer for said first gate electrode and said silicide layer for said source region or said drain region are electrically isolated by sidewall spacers formed on said side walls of said first gate electrode.

65. (Original) A method according to claim 63, wherein a gate electrode of each peripheral circuit transistor is formed of a film obtained by laminating a conductive film lying in the same layer as said first conductive film, and a second conductive film lying in the same layer as said memory gate electrode.

66. (Original) A method according to claim 63,

wherein sidewall spacers are formed on side walls of said gate electrode of the peripheral circuit transistor in said sidewall spacer forming step, and

wherein a silicide layer is formed over said gate electrode of said peripheral circuit transistor in said silicide layer forming step.

67. (Original) A method according to claim 63,

wherein said memory cell includes, in a memory cell forming region of a semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode disposed near one of said source and drain regions, a memory gate electrode disposed near the other of said source and drain regions, a first gate insulating film formed between said channel region and said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

68. – 70. (Cancelled)

71. (Currently Amended) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductive film over a memory cell forming region of a semiconductor substrate and forming an insulating film on said first conductive film;

etching said insulating film and said first conductive film to form a first ~~conductive~~ conductor pattern which serves as a first gate electrode of a memory cell;

forming a second gate electrode of said memory cell on side walls of said first ~~conductive~~ conductor pattern;

removing said insulating film over said first conductor pattern;

forming sidewall spacers, each comprised of an insulating film, in self-

alignment with side walls of said second gate electrode; and

etching said first ~~conductive~~ conductor pattern in self-alignment with respect to said sidewall spacers to form corresponding first gate electrode.

72. (Original) A method according to claim 71,

wherein a second gate insulating film is formed between said second gate electrode and said semiconductor substrate,

wherein said sidewall spacers are formed on said side walls on both sides of said second gate electrode,

wherein said second gate insulating film is formed in self-alignment with respect to said sidewall spacer on one side of said both sides, and

wherein said first gate electrode is formed in self-alignment with respect to said sidewall spacer on the other side thereof.

73. (Original) A method according to claim 71, wherein a gate electrode of each peripheral circuit transistor is formed of a film obtained by laminating a conductive film lying in the same layer as said first conductive film, and a second conductive film lying in the same layer as said memory gate electrode.

74. (Currently Amended) A method according to claim 71,

wherein said second gate insulating film includes a nonconductive charge trap film corresponding to a charge storage region,

wherein said first gate electrode constitutes a control gate electrode, and

wherein said second gate electrode constitutes a memory gate electrode and is formed on side walls of said control gate electrode through an insulating film in sidewall spacer ~~fashion~~ shape.

75. – 85. (Cancelled)

86. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 52, wherein, in the silicide layers forming step, a third silicide layer is formed on said second conductive film of said electrode structure.

87. (New) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductive film into a first conductor pattern which serves as a first gate electrode of a memory cell over a memory cell forming region of a semiconductor substrate;

forming an insulator film over side surface of said first conductor pattern and over said memory cell forming region;

forming a second conductive film over said memory cell forming region and said insulator film;

etching said second conductive film to form a second gate electrode of said memory cell on at least side surface of said first conductor pattern;

forming a sidewall spacer of an insulator material in self-alignment with side walls of said second gate electrode; and

forming a first silicide layer on said first gate electrode of said memory cell and a second silicide layer on said second gate electrode of said memory cell,

wherein said first silicide layer and said second silicide layer are electrically separated.

88. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 87, wherein, in said etching step, said second gate electrode is formed in self-alignment with said side surface of said first conductor pattern such that said second conductive film has a pattern shape of a sidewall spacer.

89. (New) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductive film into a first conductor pattern which serves as a first gate electrode of a memory cell over a memory cell forming region of a semiconductor substrate;

forming an insulator film over side surfaces of said first conductor pattern and over said memory cell forming region;

forming a second conductive film over said memory cell forming region and said insulator film;

etching said second conductive film to form a second conductor pattern in self-alignment with said surface of said first conductor pattern such that said second conductor pattern has a shape of a sidewall spacer;

removing said second conductor pattern to form a second gate electrode of said memory cell on one side of said side surfaces of said first conductor pattern;

forming sidewall spacers of an insulator material in self-alignment with side walls of said second gate electrode and in self-alignment with said side surface of

said first gate electrode; and

forming a first silicide layer on said first gate electrode of said memory cell and a second silicide layer on said second gate electrode of said memory cell,

wherein said first silicide layer and said second silicide layer are electrically separated.

90. (Currently Amended) A method of manufacturing a semiconductor integrated circuit device according to claim 89, further comprising the step of:

before said sidewall spacers forming step, forming a gate electrode of a peripheral circuit transistor,

wherein, in said sidewall spacers forming step, said sidewall spacers are formed in self-alignment with said gate electrode of said peripheral circuit transistor,

wherein, in the silicide layers forming step, a third silicide layer is formed on said gate electrode of said peripheral circuit transistor.

91. (New) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductive film over a memory cell forming region and a peripheral circuit forming region of a semiconductor substrate;

patterning said first conductive film in said memory cell forming region so as to form a first conductor pattern which serves as a first gate electrode of a memory cell;

forming an insulator film over side surface of said first conductor pattern and over said memory cell forming region;

forming a second conductive film over said memory cell forming region and

said insulator film;

etching said second conductive film to form a second conductor pattern, serving as a second gate electrode of said memory cell, in self-alignment with said first conductor pattern such that said second conductor pattern has a shape of a side wall spacer;

forming a gate electrode of a peripheral circuit transistor by patterning said first conductive film in said peripheral circuit forming region;

forming sidewall spacers of an insulator material in self-alignment with side walls of said second gate electrode, in self-alignment with said side surface of said first gate electrode and in self-alignment with side surfaces of said gate electrode of said peripheral circuit transistor; and

forming a first silicide layer on said first gate electrode of said memory cell, a second silicide layer on said second gate electrode of said memory cell and a third silicide layer on said gate electrode of said peripheral circuit transistor,

wherein said first silicide layer and said second silicide layer are electrically separated.

92. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 91,

wherein said memory cell includes, in a memory cell forming region of said semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode and a memory gate electrode disposed over said channel region, a first gate insulating film formed between said channel region and said control gate

electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

93. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 92,

wherein said peripheral circuit transistor constitutes either one of a low withstand voltage transistor operated at a power voltage, and a high withstand voltage transistor operated at a voltage higher than said power voltage, and

wherein said first gate insulating film is formed in a gate insulating film forming step for said low withstand voltage transistor.

94. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 89,

wherein said memory cell includes, in a memory cell forming region of said semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode and a memory gate electrode disposed over said channel region, a first gate insulating film formed between said channel region and said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

95. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 94,

wherein a peripheral circuit element is formed in a peripheral circuit forming region of said semiconductor substrate and includes a low withstand voltage transistor operated at a power voltage, and a high withstand voltage transistor operated at a voltage higher than said power voltage, and

wherein said gate insulating film is formed in a gate insulating film forming step for said low withstand voltage transistor.

96. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 87,

wherein said memory cell includes, in a memory cell forming region of said semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode and a memory gate electrode disposed over said channel region, a first gate insulating film formed between said channel region and said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

97. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 96,

wherein a peripheral circuit element is formed in a peripheral circuit forming region of said semiconductor substrate and includes a low withstand voltage transistor operated at a power voltage, and a high withstand voltage transistor operated at a voltage higher than said power voltage, and

wherein said gate insulating film is formed in a gate insulating film forming step for said low withstand voltage transistor.

98. (New) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductor pattern which serves as a first gate electrode of a memory cell over a memory cell forming region of a semiconductor substrate;

forming an insulator film over side surface of said first conductor pattern and over said memory cell forming region;

forming a second gate electrode of said memory cell in self-alignment with said side surface of said first conductor pattern such that said second gate electrode has a shape of a sidewall spacer and such that said insulator film is formed between said first conductor pattern and said second gate electrode;

forming a side wall spacer of an insulator material in self-alignment with side walls of said second gate electrode; and

forming a first silicide layer on said first gate electrode of said memory cell and a second silicide layer on said second gate electrode of said memory cell,

wherein said first silicide layer and said second silicide layer are electrically separated.

99. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 98,

wherein said memory cell includes, in a memory cell forming region of said semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode and a memory gate electrode disposed over said channel region, a first gate insulating film formed between said channel region and said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

100. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 99,

wherein a peripheral circuit element is formed in a peripheral circuit forming region of said semiconductor substrate and includes a low withstand voltage transistor operated at a power voltage, and a high withstand voltage transistor operated at a voltage higher than said power voltage, and

wherein said gate insulating film is formed in a gate insulating film forming step for said low withstand voltage transistor.

101. (New) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductor pattern which serves as a first gate electrode of a memory cell over a memory cell forming region of a semiconductor substrate;

forming an insulator film over side surface of said first conductor pattern and over said memory cell forming region;

selectively forming a second gate electrode of said memory cell in self-alignment with one side surface of said first conductor pattern such that said second gate electrode has a shape of a sidewall spacer and such that said insulator film is formed between said first conductor pattern and said second gate electrode;

forming sidewall spacers of an insulator material in self-alignment with side walls of said second gate electrode, in self-alignment with other side surface of said first conductor pattern; and

forming a first silicide layer on said first gate electrode of said memory cell and a second silicide layer on said second gate electrode of said memory cell,

wherein said first silicide layer and said second silicide layer are electrically separated.

102. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 101,

wherein said memory cell includes, in a memory cell forming region of said semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode and a memory gate electrode disposed over said channel region, a first gate insulating film formed between said channel region and said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

103. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 102,

wherein a peripheral circuit element is formed in a peripheral circuit forming region of said semiconductor substrate and includes a low withstand voltage transistor operated at a power voltage, and a high withstand voltage transistor operated at a voltage higher than said power voltage, and

wherein said gate insulating film is formed in a gate insulating film forming step for said low withstand voltage transistor.

104. (New) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductive film over a memory cell forming region and a peripheral circuit forming region of a semiconductor substrate;

patterning said conductive film in said memory cell forming region to form a first conductor pattern which serves as a first gate electrode of a memory cell;

forming an insulator film over side surface of said first conductor pattern and over said memory cell forming region;

forming a second gate electrode of said memory cell in self-alignment with said side surface of said first conductor pattern such that said second gate electrode has a shape of a side wall spacer and such that said insulator film is formed between said first conductor pattern and said second gate electrode;

forming a gate electrode of a peripheral circuit transistor by patterning said first conductive film in said peripheral circuit forming region;

forming sidewall spacers of an insulator material in self-alignment with side

walls of said second gate electrode, in self-alignment with said side surfaces of said first gate electrode and in self-alignment with side surfaces of said gate electrode of said peripheral circuit transistor; and

forming a first silicide layer on said first gate electrode of said memory cell, a second silicide layer on said second gate electrode of said memory cell and a third silicide layer on said gate electrode of said peripheral circuit transistor,

wherein said first silicide layer and said second silicide layer are electrically separated.

105. (New) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductive film over a memory cell forming region and a peripheral circuit forming region of a semiconductor substrate;

patterning said conductive film in said memory cell forming region to form a first conductor pattern which serves as a first gate electrode of a memory cell;

forming an insulator film over side surface of said first conductor pattern and over said memory cell forming region;

selectively forming a second gate electrode of said memory cell in self-alignment with one side surface of said first conductor pattern such that said second gate electrode has a shape of a sidewall spacer and such that said insulator film is formed between said first conductor pattern and said second gate electrode;

forming a gate electrode of a peripheral circuit transistor by patterning said first conductive film in said peripheral circuit forming region;

forming sidewall spacers of an insulator material in self-alignment with said side walls of said second gate electrode, in self-alignment with other side surface of

said first conductor pattern and in self-alignment with side surfaces of said gate electrode of said peripheral circuit transistor; and

wherein said first silicide layer and forming a first silicide layer on said first gate electrode of said memory cell, a second silicide layer on said second gate electrode of said memory cell and a third silicide layer on said gate electrode of said peripheral circuit transistor,

said second silicide layer are electrically separated.

106. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 104,

wherein said memory cell includes, in a memory cell forming region of said semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode and a memory gate electrode disposed over said channel region, a first gate insulating film formed between said channel region and said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

107. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 106,

wherein said peripheral circuit transistor constitutes either one of a low and a high withstand voltage transistor formed in said peripheral circuit-forming region, and

wherein said firsts gate insulating film is formed in a gate insulating film forming step for said low withstand voltage transistor.

108. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 105,

wherein said memory cell includes, in a memory cell forming region of said semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode and a memory gate electrode disposed over said channel region, a first gate insulating film formed between said channel region and said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

109. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 108,

wherein said peripheral circuit transistor constitutes either one of a low and a high withstand voltage transistor formed in said peripheral circuit-forming region, and

wherein said firsts gate insulating film is formed in a gate insulating film forming step for said low withstand voltage transistor.

110. (New) A method of manufacturing a semiconductor integrated circuit

device, comprising steps of:

forming a first gate electrode of a memory cell over a memory cell forming region of a semiconductor substrate;

forming an insulator film over side surface of said first gate electrode and over said memory cell forming region;

forming a second gate electrode of said memory cell in self-alignment with said side surface of said first gate electrode such that said second gate electrode has a shape of a sidewall spacer and such that said insulator film is formed between said first gate electrode and said second gate electrode;

forming a sidewall spacer of an insulator material in self-alignment with side walls of said second gate electrode;

forming a first silicide layer on said first gate electrode of said memory cell and a second silicide layer on said second gate electrode of said memory cell,

wherein said first silicide layer and said second silicide layer are electrically separated.

111. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 110,

wherein said memory cell includes, in a memory cell forming region of said semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode and a memory gate electrode disposed over said channel region, a first gate insulating film formed between said channel region and said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

112. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 111,

wherein a peripheral circuit element is formed in a peripheral circuit forming region of said semiconductor substrate and includes a low withstand voltage transistor operated at a power voltage, and a high withstand voltage transistor operated at a voltage higher than said power voltage, and

wherein said gate insulating film is formed in a gate insulating film forming step for said low withstand voltage transistor.

113. (New) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first gate electrode of a memory cell over a memory cell forming region of a semiconductor substrate;

forming an insulator film over side surface of said first gate electrode and over said memory cell forming region;

forming a second gate electrode of said memory cell in self-alignment with said side surface of said first gate electrode such that said second gate electrode has a shape of a sidewall spacer and such that said insulator film is formed between said first gate electrode and said second gate electrode;

forming a sidewall spacer of an insulator material in self-alignment with side walls of said second gate electrode; and

forming a first silicide layer on said first gate electrode of said memory cell

and a second silicide layer on said second gate electrode of said memory cell,

wherein a height of said first gate electrode is different from a height of said second gate electrode, and

wherein said first silicide layer and said second silicide layer are electrically separated.

114. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 113,

wherein said memory cell includes, in a memory cell forming region of said semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode and a memory gate electrode disposed over said channel region, a first gate insulating film formed between said channel region and said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

115. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 114,

wherein a peripheral circuit element is formed in a peripheral circuit forming region of said semiconductor substrate and includes a low withstand voltage transistor operated at a power voltage, and a high withstand voltage transistor operated at a voltage higher than said power voltage, and

wherein said gate insulating film is formed in a gate insulating film forming

step for said low withstand voltage transistor.

116. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 105, wherein a height of said first gate electrode is different from a height of said second gate electrode.

117. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 104, wherein a height of said first gate electrode is different from a height of said second gate electrode.

118. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 101, wherein a height of said first gate electrode is different from a height of said second gate electrode.

119. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 98, wherein a height of said first gate electrode is different from a height of said second gate electrode.

120. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 91, wherein a height of said first gate electrode is different from a height of said second gate electrode.

121. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 89, wherein a height of said first gate electrode is different from a height of said second gate electrode.

122. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 87, wherein a height of said first gate electrode is different from a height of said second gate electrode.

123. (New) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first gate electrode of a memory cell over a memory cell forming region of a semiconductor substrate;

forming an insulator film over one of side surfaces of said first gate electrode and over said memory cell forming region;

forming a second gate electrode of said memory cell in self-alignment with said one of side surfaces of said first gate electrode such that said second gate electrode has a shape of a sidewall spacer and such that said insulator film is formed between said first gate electrode and said second gate electrode; and

forming sidewall spacers of an insulator material in self-alignment with side walls of said second gate electrode and in self-alignment with other of said side surfaces of said first gate electrode.

124. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 123,

wherein a peripheral circuit element is formed in a peripheral circuit forming region of said semiconductor substrate and includes a low withstand voltage transistor operated at a power voltage, and a high withstand voltage transistor

operated at a voltage higher than said power voltage, and

wherein said gate insulating film is formed in a gate insulating film forming step for said low withstand voltage transistor.

125. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 124,

wherein said peripheral circuit element includes a low withstand voltage transistor operated at a power voltage, and a high withstand voltage transistor operated at a voltage higher than said power voltage, and

wherein said first gate insulating film is formed in a gate insulating film forming step for said low withstand voltage transistor.

126. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 123, wherein a height of said first gate electrode is different from a height of said second gate electrode.

127. (New) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first gate electrode of a memory cell over a memory cell forming region of a semiconductor substrate;

forming an insulator film over side surface of said first gate electrode and over said memory cell forming region;

forming a second gate electrode of said memory cell in self-alignment with said side surface of said first gate electrode such that said second gate electrode has a shape of a sidewall spacer and such that said insulator film is formed between

said first gate electrode and said second gate electrode;

forming a gate electrode of a peripheral circuit transistor in a peripheral circuit forming region;

forming sidewall spacers of an insulator material in self-alignment with side walls of said second gate electrode and in self-alignment with side surfaces of said gate electrode of said peripheral circuit transistor; and

forming a first silicide layer on said first gate electrode of said memory cell, a second silicide layer on said second gate electrode of said memory cell and a third silicide layer on said gate electrode of said peripheral circuit transistor,

wherein said first silicide layer and said second silicide layer are electrically separated.

128. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 127,

wherein said memory cell includes, in a memory cell forming region of said semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode and a memory gate electrode disposed over said channel region, a first gate insulating film formed between said channel region and said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

129. (New) A method of manufacturing a semiconductor integrated circuit

device according to claim 128,

wherein said peripheral circuit transistor constitutes either one of a low and a high withstand voltage transistor formed in said peripheral circuit-forming region, and

wherein said firsts gate insulating film is formed in a gate insulating film forming step for said low withstand voltage transistor.

130. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 127, wherein a height of said first gate electrode is different from a height of said second gate electrode.

131. (New) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first gate electrode of a memory cell over a memory cell forming region of a semiconductor substrate;

forming an insulator film over one of side surfaces of said first gate electrode and over said memory cell forming region;

forming a second gate electrode (8) of said memory cell in self-alignment with said one of side surfaces of said first gate electrode such that said second gate electrode has a shape of a sidewall spacer and such that said insulator film is formed between said first gate electrode and said second gate electrode;

forming a gate electrode of a peripheral circuit transistor in a peripheral circuit forming region;

forming sidewall spacers of an insulator material in self-alignment with side walls of said second gate electrode and in self-alignment with side surfaces of said

gate electrode of said peripheral circuit transistor; and

forming a first silicide layer on said first gate electrode of said memory cell, a second silicide layer on said second gate electrode of said memory cell and a third silicide layer on said gate electrode of said peripheral circuit transistor,

wherein said first silicide layer and said second silicide layer are electrically separated.

132 (New) A method of manufacturing a semiconductor integrated circuit device according to claim 131,

wherein said memory cell includes, in a memory cell forming region of said semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode and a memory gate electrode disposed over said channel region, a first gate insulating film formed between said channel region and said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

133. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 132,

wherein said peripheral circuit transistor constitutes either one of a low and a high withstand voltage transistor formed in said peripheral circuit-forming region, and

wherein said firsts gate insulating film is formed in a gate insulating film

forming step for said low withstand voltage transistor.

134. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 131, wherein a height of said first gate electrode is different from a height of said second gate electrode.

135. (New) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductor pattern serving as a gate electrode of a memory cell over a memory cell forming region of a semiconductor substrate and a second conductor pattern over a peripheral circuit forming region of said substrate;

forming an insulator film over side surface of said first gate electrode and over said memory cell forming region;

forming a second gate electrode of said memory cell in self-alignment with said side surface of said first gate electrode such that said second gate electrode has a shape of a sidewall spacer and such that said insulator film is formed between said first gate electrode and said second gate electrode,

wherein in said second gate electrode forming step, a third conductor pattern is formed over said second conductor pattern,

forming side wall spacers of an insulator material in self-alignment with side walls of said second gate electrode; and

forming a first silicide layer on said first gate electrode of said memory cell and a second silicide layer on said second gate electrode of said memory cell,

wherein said first silicide layer and said second silicide layer are electrically separated.

136. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 135,

wherein in said sidewall spacers forming step, sidewall spacers of said insulator material are formed in self-alignment with side walls of said third conductor pattern and said second conductor pattern,

wherein in said silicide layers forming step, a third silicide layer is formed on said third conductor pattern, and

wherein said third conductor pattern and said second conductor pattern serve as a gate electrode of a transistor of a peripheral circuit.

137. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 135,

wherein said memory cell includes, in a memory cell forming region of said semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode and a memory gate electrode disposed over said channel region, a first gate insulating film formed between said channel region and said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode..

138. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 137,

wherein a peripheral circuit element is formed in a peripheral circuit forming region of said semiconductor substrate and includes a low withstand voltage transistor operated at a power voltage, and a high withstand voltage transistor operated at a voltage higher than said power voltage, and

wherein said first gate insulating film is formed in a gate insulating film forming step for said low withstand voltage transistor.

139. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 87, wherein, in said silicide layers forming step, a third silicide layer is formed on a semiconductor region serving as a source or drain region such that said third silicide layer is formed in self-alignment with said side wall spacer.

140. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 89,

wherein, in said silicide layers forming step, a third silicide layer and a fourth silicide layer are formed on a first semiconductor region and a second semiconductor region, respectively, such that said third silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said second gate electrode and such that said fourth silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said first gate electrode, and

wherein a channel forming region is formed between said first semiconductor region and said second semiconductor region.

141. (New) A method of manufacturing a semiconductor integrated circuit

device according to claim 91,

wherein, in said silicide layers forming step, a fourth silicide layer, a fifth silicide layer and a sixth silicide layer are formed on a first semiconductor region, a second semiconductor region and a third semiconductor region, respectively, such that said fourth silicide layer is formed in self-alignment with said sidewall spacer formed on said sidewall of said second gate electrode, such that said fifth silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said first gate electrode and such that said sixth silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said gate electrode of said peripheral circuit transistor, and

wherein a channel forming region is formed between said first semiconductor region and said second semiconductor region.

142. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 98,

wherein, in said side wall spacer forming step, a further sidewall spacer is formed in self-alignment with a side surface of said first gate electrode,

wherein, in said silicide layer forming step, a third silicide layer and a fourth silicide layer are formed on a first semiconductor region and a second semiconductor region, respectively, such that said third silicide layer is formed in self-alignment with said side wall spacer formed on said side wall of said second gate electrode and such that said fourth silicide layer is formed in self-alignment with said further sidewall spacer formed on said side wall of said first gate electrode, and

wherein a channel forming region is formed between said first semiconductor

region and said second semiconductor region.

143. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 101,

wherein, in said silicide layer forming step, a third silicide layer and a fourth silicide layer are formed on a first semiconductor region and a second semiconductor region, respectively, such that said third silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said second gate electrode and such that said fourth silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said first gate electrode, and

wherein a channel forming region is formed between said first semiconductor region and said second semiconductor region.

144. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 104,

wherein, in said silicide layer forming step, a third silicide layer and a fourth silicide layer are formed on a first semiconductor region and a second semiconductor region, respectively, such that said third silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said second gate electrode and such that said fourth silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said first gate electrode, and

wherein a channel forming region is formed between said first semiconductor region and said second semiconductor region.

145. (New) A method of manufacturing a semiconductor integrated circuit

device according to claim 105,

wherein, in said silicide layer forming step, a third silicide layer and a fourth silicide layer are formed on a first semiconductor region and a second semiconductor region, respectively, such that said third silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said second gate electrode and such that said fourth silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said first gate electrode, and

wherein a channel forming region is formed between said first semiconductor region and said second semiconductor region.

146. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 110,

wherein, in said sidewall spacer forming step, a further sidewall spacer is formed in self-alignment with a side surface of said first gate electrode, and

wherein, in said silicide layer forming step, a third silicide layer and a fourth silicide layer are formed on a first semiconductor region and a second semiconductor region, respectively, such that said third silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said second gate electrode and such that said fourth silicide layer is formed in self-alignment with said further sidewall spacer formed on said side wall of said first gate electrode, wherein a channel forming region is formed between said first semiconductor region and said second semiconductor region.

147. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 123,

wherein, in said silicide layer forming step, a third silicide layer and a fourth silicide layer are formed on a first semiconductor region and a second semiconductor region, respectively, such that said third silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said second gate electrode and such that said fourth silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said first gate electrode, and

wherein a channel forming region is formed between said first semiconductor region and said second semiconductor region.

148. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 127, wherein, in said silicide layer forming step, a fourth silicide layer and a fifth silicide layer are formed on a first semiconductor-region and a second semiconductor region, respectively, such that said fourth silicide layer is formed in self-alignment with said sidewall spacer formed on said sidewall of said second gate electrode and such that said fifth silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said gate electrode of said peripheral circuit.

149. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 131, wherein, in said silicide layer forming step, a fourth silicide layer and a fifth silicide layer are formed on a first semiconductor region and a second -semiconductor region, respectively, such that said fourth silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said second gate electrode and such that said fifth silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said gate electrode

of said peripheral circuit.

150. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 135,

wherein, in said sidewall spacer forming step, a further sidewall spacer is formed in self-alignment with a side surface of said first gate electrode,

wherein, in said silicide layer forming step, a third silicide layer and a fourth silicide layer are formed on a first semiconductor region and a second semiconductor region, respectively, such that said third silicide layer is formed in self-alignment with said sidewall spacer formed on said side wall of said second gate electrode and such that said fourth silicide layer is formed in self-alignment with said further sidewall spacer formed on said side wall of said first gate electrode, and

wherein a channel forming region is formed between said first semiconductor region and said second semiconductor region.